IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble et al.	Examiner: Michael Trinh	
Serial No.:	09/551,027	Group Art Unit: 2822	
Filed:	April 17, 2000	Docket: 303.379US2	
Title:	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR		

25/6 Amdt 6-23-03 A Walk

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on September 24, 2002. Please amend the above-identified patent application as follows.

IN THE DRAWINGS

Applicant notices a typographical error in FIG. 3. Reference number 212 used for the substrate is already used for a word line. Therefore, Applicant proposes an amendment to FIG. 3 to change 212 of the substrate to 201. Applicant requests an approval from the Examiner for the amendment and will submit formal drawings after the claims are allowed.

IN THE SPECIFICATION

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the term's "a single unbonded substrate" mentioned in the claims (e.g. claim 20), but not in the specification.

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning at page 9, line 26 is amended as follows:

Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into first source/drain region 206, body region 208, and second source/drain region 210 to form access transistor 211. Pillar 204 extends vertically